**DIGITAL COMMUNICATION LAB REPORT**



**DELTA MODULATION**

( *Hardware* )

***Submitted by –***

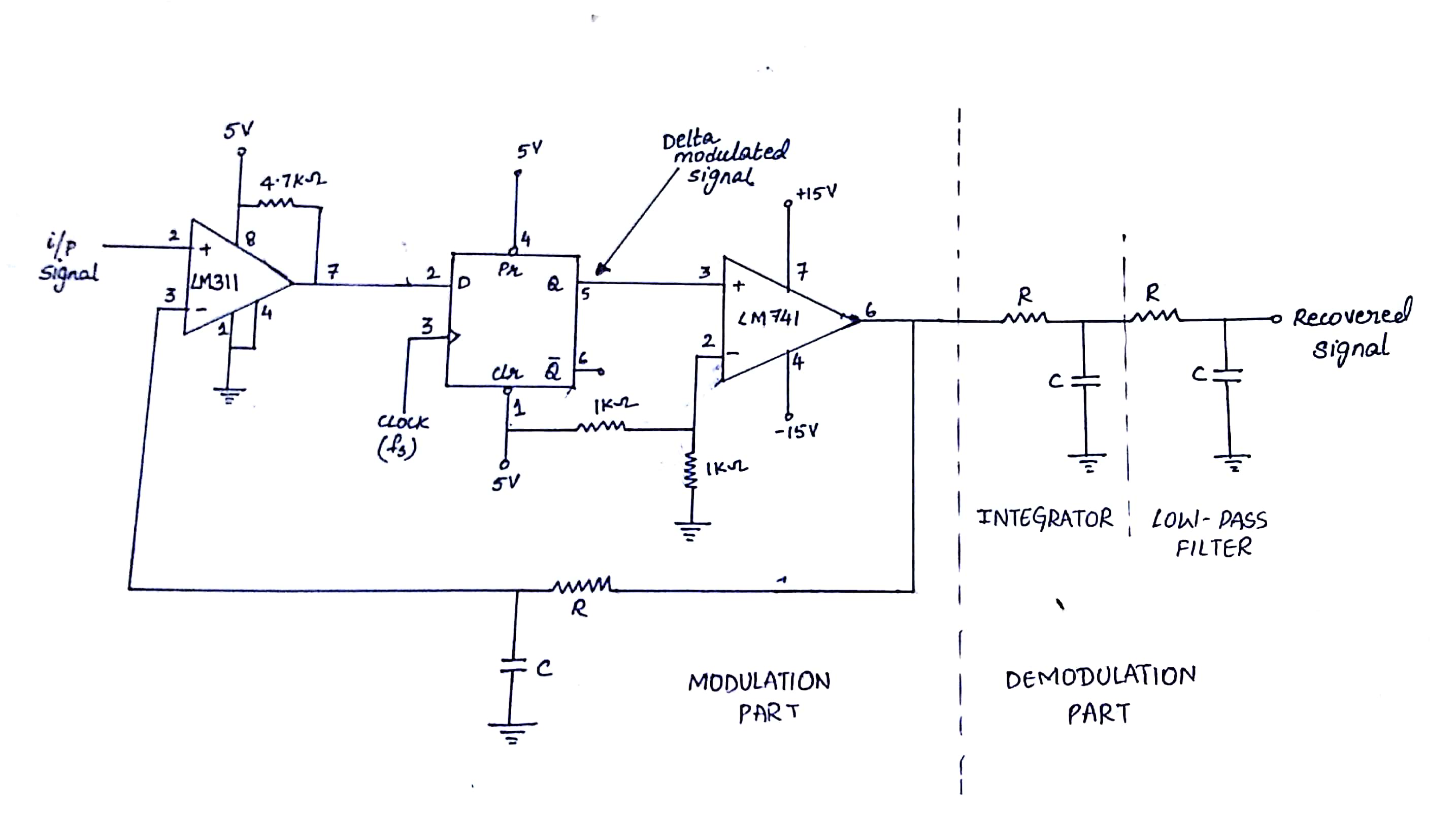
SOWMYA BITRA (B150821EC)

TEJASWI MANUKONDA (B150571EC)

V. LAKSHMI PRASANNA (B150738EC)

VUNDAVALLI ASWINI (B150519EC)

**CIRCUIT DIAGRAM:**



**DESIGN:**

Given input

Sampling frequency

To avoid slope overload error,

Choosing  **∆=0.5**

Using this value of ∆ to design time constant of integrator,

**AIM:**

Setup a circuit to implement delta modulation and observe the modulated output for a sinusoidal input wave.

**COMPONENTS REQUIRED:**

1. IC7474 (D Flip-Flop)
2. IC741
3. IC311
4. Resistors
5. Capacitors
6. Breadboard

**THEORY:**

Differential pulse-code modulation (DPCM) is a modulation technique where the difference between successive samples are encoded into n-bit data streams. Delta modulation is the simplest form of DPCM, where samples are encoded using one bit. It is an analog-to-digital and digital-to-analog signal conversion technique where quality is not of primary importance.

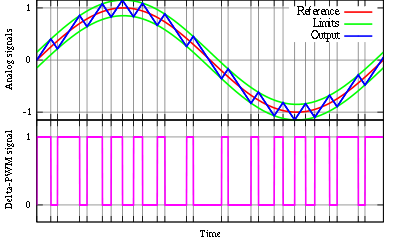
***Modulation procedure:***

* The analog signal is approximated with a series of segments.
* Each segment of the approximated signal is compared to the original analog wave to determine the increase or decrease in relative amplitude. The decision process for establishing the state of successive bits is determined by this comparison.
* Only the change of information is sent, that is, only an increase or decrease of the signal amplitude from the previous sample is sent whereas a no-change condition causes the modulated signal to remain at the same 0 or 1 state of the previous sample.
* To achieve high signal-to-noise ratio, delta modulation must use oversampling techniques, that is, the analog signal is sampled at a rate several times higher than the Nyquist rate.

***Two main issues with delta modulation:***

* ***Slope overload error***: When the designed step size of the DM circuit is unable to keep up with sudden variations in the input, the output lags behind the input, causing it to get distorted more and more. This can be avoided by selecting a suitable step size considering the maximum rate of change of the input
* ***Granular noise***: This occurs when the signal is more or less remaining steady. Now the feedback signal can be below or above the input voltage, as the next bit is sent the output increases or decreases w.r.t the step size, again repeating this process causing the output to oscillate (square wave like output). Adaptive step size control can be used to avoid this problem.

**EXPECTED WAVEFORMS:**



**OBSERVED WAVEFORMS:**

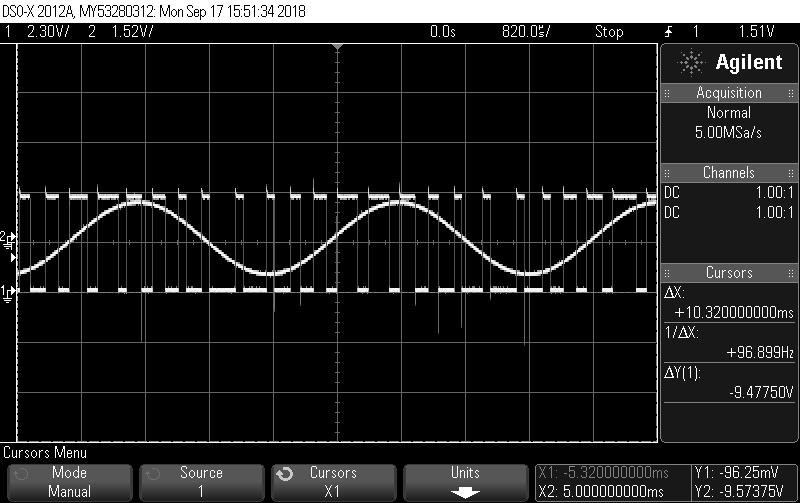
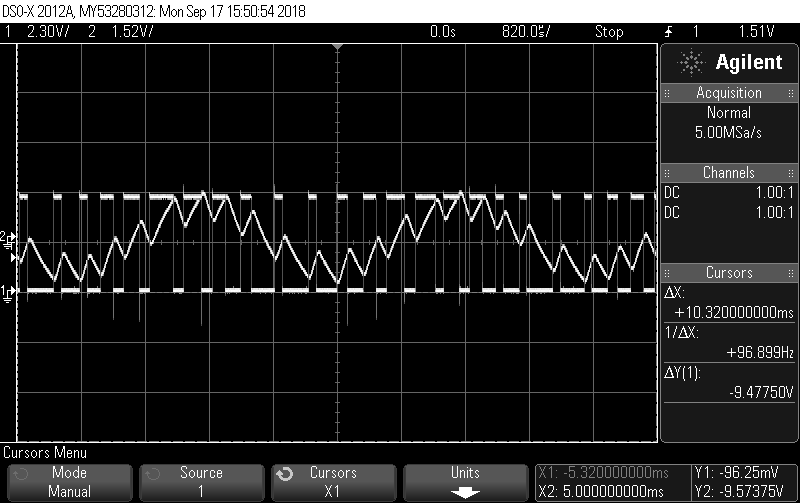
 

Fig 1: Input sinusoidal and delta modulated Fig 2: Delta modulated signal and integrator

signal. output.

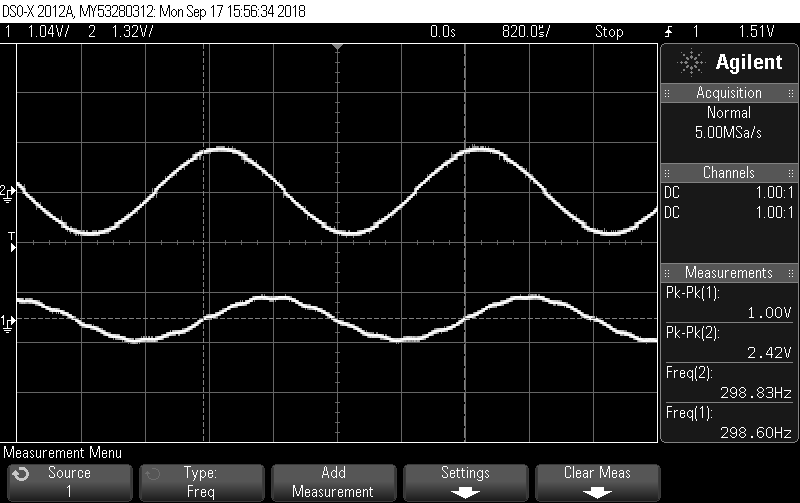


Fig 3: Input sinusoidal signal and demodulated signal.

**PROCEDURE:**

1. Design the circuit for the required signal and hence obtain the step size required for the delta modulated signal.
2. Set up comparator circuit using IC741 to compare the input signal (non-inverting terminal) to the feedback signal (decoded DM signal).
3. The output of the comparator is level corrected (TTL voltages) using a diode and voltage divider circuit and sent to a D flip flop for sampling and holding and to introduce a 1-bit delay.
4. This DM sequence is sent to integrator circuit, and after attenuating it to match the required step size specifications. The integrator output is fed back to the comparator to close the loop.

**INFERENCES:**

It was observed that for optimal performance the step size should be as small as possible, but large enough to avoid any slope overload errors at the given input signal frequency. But higher step sizes can cause granular noise when the output is a constant. Also, for a more accurate recovery of the original signal the sampling rate should be large (more than 10 times the input signal frequency).

**RESULT:**

A Delta modulator was designed and implemented using discrete hardware components, and its output was observed and verified.